AN-432 A
A MONOLITHIC INTEGRATED
FM STEREO DECODER SYSTEM

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INTRODUCTION

The use of integrated circuits in high quality FM receivers is already a fact. As the trend continues to a more extensive use of these units, the development of an integrated circuit FM stereo decoder becomes most desirable.

In practice, the integration of a discrete multiplex circuit cannot be restricted to the realization of the different stages involved in the stereo decoding action, but should consider the incorporation, in the same chip, of some of the auxiliary circuits so often used in FM stereo design. The number and type of these auxiliary circuits vary from one receiver to another. In some of them it reduces to a simple lamp indicator, in others it evolves into a more sophisticated approach where automatic, as well as manual selection for the muting and the stereo-monaural mode are available.

A comprehensive solution of all these circuit problems is given by either the MC1304 or the MC1305 versions of the IC multiplex. These two ICs consist of two different functional blocks, one containing the stereo decoder, the other containing three auxiliary circuits providing muting, stereo-monaural selection, and stereo lamp indication. The MC1305, in particular, has provision to incorporate an external variable resistor (pin 9) to adjust the channel separation. (Figure 3)

These auxiliary circuits can be combined in several ways, giving the designer a choice of several combinations which meet personal design preferences. Muting between stations, automatic switching to monaural reception for weak stereo signals, and "stereo select" action, are some of these options.
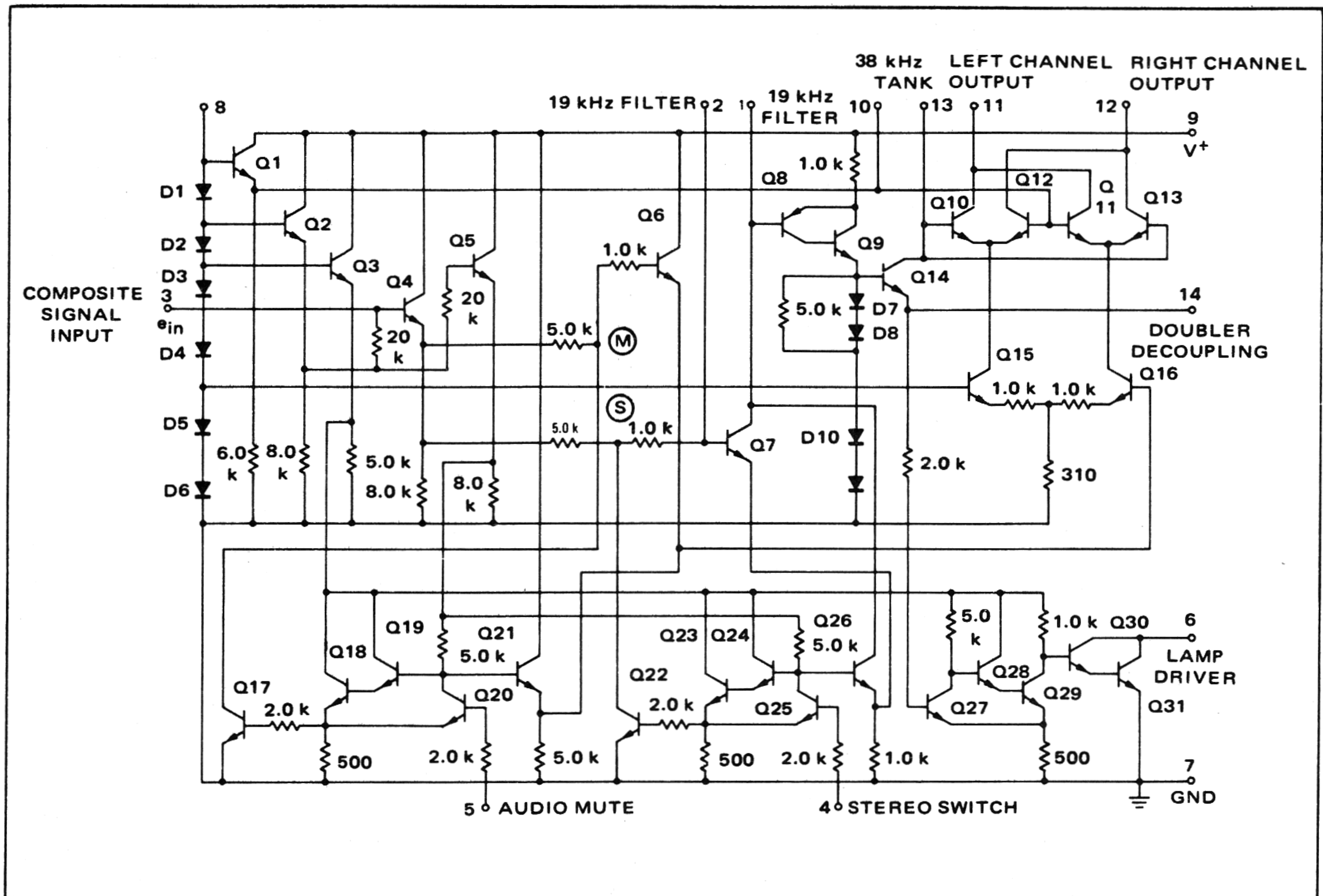
Special care has been taken to assure the quality of

FIGURE 1 — MC1304 Circuit Schematic

FIGURE 2 — Simplified Diagram of Stereo Decoder Portion

these auxiliary circuits. The stereo lamp indicator in particular has a built-in hysteresis that makes it possible to tune a stereo station without flickering.

The ICs feature excellent channel separation across the entire audio range (in excess of 30 dB); good ultrasonic rejection (in excess of 20 dB at 38 kHz); low THD content at the output (less than 1%*) and excellent SCA immunity for services using a 67 kHz subcarrier (in excess of 50 dB without the use of an external trap).

Power supply requirements are mainly determined by the lamp indicator circuit, which handles up to 40 mA. The rest of the IC requires 10 mA at 8.5 V.

FM STEREO DECODER CIRCUIT OPERATION

The complete circuit diagram of the MC1304 is shown in Figure 1. (No functional differences exist between the MC1304 and 1305 versions.) For the sake of simplicity, Figure 2 shows only the FM stereo decoder portion neglecting the auxiliary switching and biasing circuits.

The composite signal from the FM detector is coupled to the base of Q4, via C1. This capacitor, in conjunction with the input impedance of the integrated circuit, gives an R-C time constant which will determine the minimum

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*NOTE: If the THD (stereo mode) of audio frequencies higher than 3 kHz is being evaluated using a distortion analyzer, values in excess of 1% will be recorded. This apparent discrepancy is due to the presence of spurious frequency by-products (beating between the 19 kHz pilot and the audio information) that fall in the harmonic frequency spectrum of the incoming audio signal, and are not attenuated by the frequency roll-off of the de-emphasis network. If a wave analyzer is used, a true reading for the THD, as well as the incidence of these by-products is obtained.

frequency response in the circuit, and consequently, the highest channel separation obtainable at the low frequency end of the audio spectrum.

In receivers where a strong high frequency roll-off of the composite signal is expected, parallel R-C compensation could be used in series with the input to improve channel separation at the high frequency end.

Transistor Q4 is used as an emitter follower to provide the high input impedance level needed in the IC to avoid any serious loading of the FM detector. Actually, due to the high degree of feedback provided by its associated emitter resistance, the input impedance is determined primarily by the 20 kilohm resistor connected between its base and the biasing network. The output of Q4 is fed to the detector, via Q6, another emitter follower stage, and to Q7, the 19 kHz amplifier.

For the recovery of the 19 kHz pilot signal, a parallel tuned circuit is used across the input of Q7. To further increase the overall selectivity of the circuit at 19 kHz, thus improving its noise immunity, a second high-Q resonant circuit is used at the output of this stage.

The combination Q8–Q9 acts as a high gain PNP transistor which couples the 19 kHz signal into the base of Q14, the frequency doubler, which has a high-Q parallel-tuned circuit for its collector load. The coil of this tuned circuit is tapped down to reflect a low impedance across the output of Q14. A 10:1 transformation sets an output impedance not higher than 2 kilohm, avoiding saturation of Q14. If higher impedances are used, the time symmetry of the 38 kHz signal could be lost and a severe degradation of the channel separation is to be expected.

A synchronous detector is used to demodulate the stereophonic information. When a stereo signal reaches the detector, the 38 kHz voltage developed across the doubler load will switch the transistors of the two upper differential pairs ON and OFF, according to the polarity of the driving signal. A time multiplexing of the composite stereo signal takes place (see Appendices I and II) at a
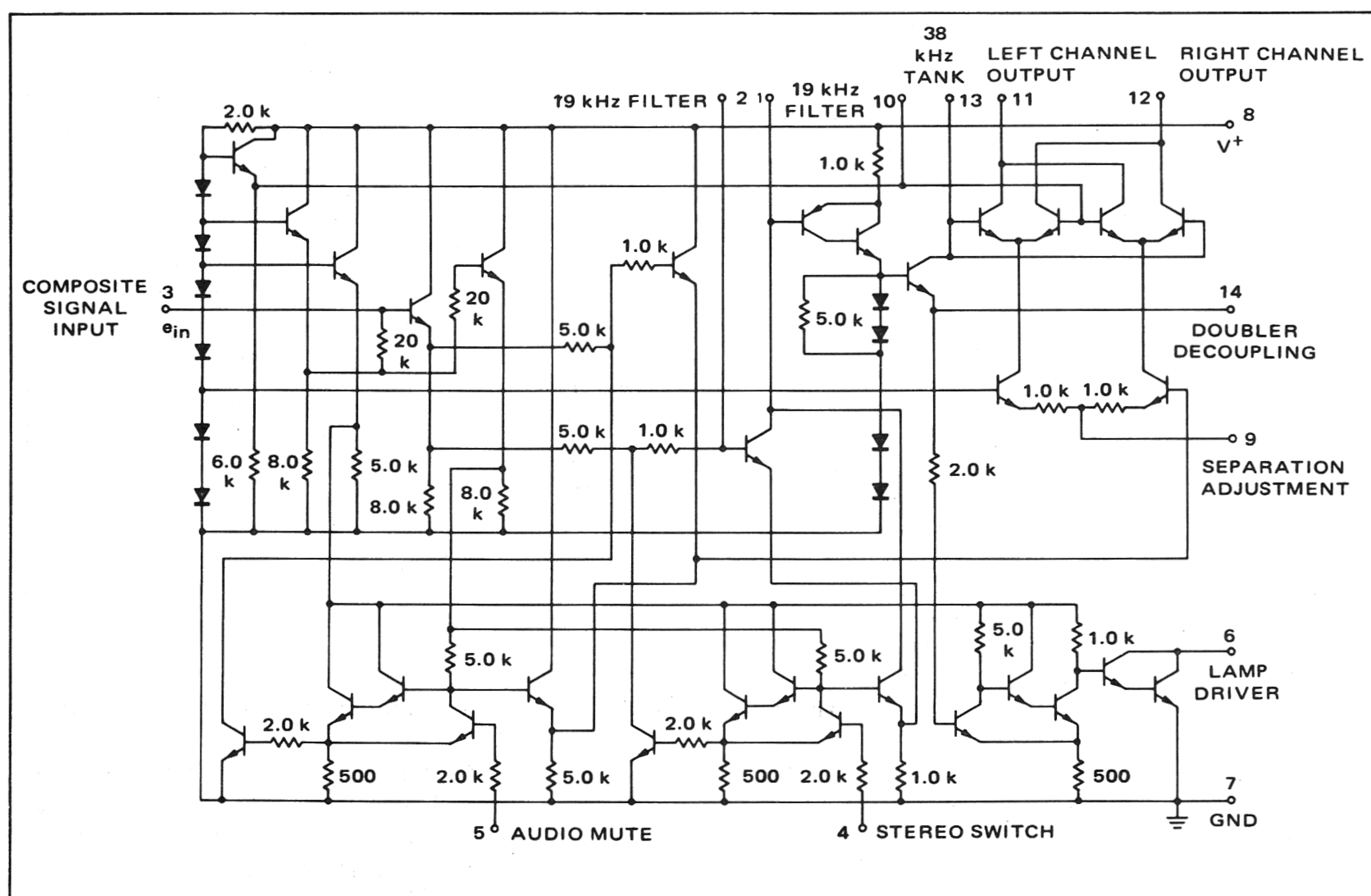
FIGURE 3 — MC1305 Circuit Schematic

38 kHz rate, permitting the separation of the left and right channel information.

The three resistors (R1, R2, and R3) associated with the lower pair in the synchronous detector help increase the channel separation by adding matrixing action to the decoding process (see Appendix II). As it was stated in the introduction, R3 becomes an external adjustable resistor.

An additional feature of this demodulator is its capability of cancelling, to a large extent, the ultrasonic components that otherwise would be present at the audio outputs when a stereo signal is being processed. This cancellation is obtained by combining two equal but opposite in-phase voltage variations in a given load, by cross coupling the collectors in the two upper pairs.

If the time symmetry of the 38 kHz square wave driving the detector is maintained by choosing the proper ac load for the doubler, no even harmonics of the 38 kHz drive will be present in the detector and, consequently, no SCA intermodulation will take place.

As could be expected, the degree of time-symmetry that can be obtained in a practical circuit has certain limitations. Even so, the minimum attenuation achieved in this circuit for any one of the SCA intermodulation products* (Table III) is not lower than 55 dB below the 1 kHz output level, obtained with an input signal of

200 mV(rms) (L = 0; R = 1 or vice versa).

This effective 67 kHz "built-in" trapping action makes it unnecessary to use an external SCA trap and, consequently, better channel separation is available at the high end of the audio range at lower cost.

The detector can also handle a monaural signal. In this case, the two upper differential pairs (Q10–Q12, and Q11–Q13) will be inactive and the monaural signal fed to the lower pair will be developed across the output load resistors, R_L and R_R, as for stereo (Figure 2).

The overall gain of the decoder could be made a function of the B+ voltage being used. When an 8.5 V power supply is used, the gain is very close to unity. If more gain is needed, the B+ voltage and the values used for R_L and R_R could be increased. The associated capacitors will have to be modified to preserve the 75 μs de-emphasis required by the system. In particular, if a 14 V B+ voltage is selected, $R_L = R_R = 10$ kilohm and the overall gain will be around 4.5 dB above the level obtained using an 8.5 V supply. A 6 dB lower output is to be expected when a stereo signal is processed using the monaural mode of operation.

AUXILIARY CIRCUITS

Three auxiliary circuits are incorporated in the MC1304. Each consists of an electronic switch associated with a Schmitt Trigger. This provides fast and positive switching after the respective threshold levels have been reached.

Muting and Stereo/Monaural Switches. Both the muting and the stereo/monaural switch are "normally closed"

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*NOTE: See reference.

switches so they will open only if a minimum dc voltage is supplied to the proper terminal. The values required to turn the switches ON and OFF are given in Table IV.

If no voltage is supplied to these circuits, the muting switch and the stereo/monaural switch will ground points Ⓜ and Ⓢ (Figure 2) through Q17 and Q22, respectively.

To avoid overloading in these switching transistors, points Ⓜ and Ⓢ each have a 5.0 kilohm resistor in series with the driving source.

An effective ac grounding of the signal at Ⓜ makes it possible to obtain a high level of audio attenuation at the output of the decoder. This muting action can be achieved automatically. If this is the case, the dc voltages needed to turn the switch ON and OFF become a function of the S/N level of the incoming RF signal, as mentioned in "Circuit Considerations".

The Stereo Lamp Indicator. The stereo lamp indicator is connected internally and represents a "normally open" switch in series with the bulb and the power supply.

When a stereo signal is received, the dc voltage on the emitter of Q14 rises, triggering the switch ON.

The 19 kHz pilot level needed at the input of the IC to turn the stereo lamp indicator ON (pilot sensitivity) can be adjusted, within a certain range, by adding a resistor, R_A, in series with pin 1. This resistor will change the threshold level of the combination Q8–Q9. In a typical unit, the pilot sensitivity is increased by a factor of 2:1 by changing the value of the series resistance from 0 to 240 ohm (see Data Sheet).

The dc voltages required to turn this switch ON and OFF differ by 2 mV on the average, which is the built-in hysteresis mentioned before. The hysteresis assures a definite ON condition once the threshold level of the switch has been reached.

Functional Arrangements of the Auxiliary Circuits. The three auxiliary circuits can be combined in various ways to form different functional arrangements. Specific circuit considerations are discussed in a following section.

One of these arrangements has already been mentioned when referring to the automatic mute action. In this case only one switch has been considered at a time.

Other schemes, combining the action of two switches, are also available; for example, the mute switch could be driven using the dc voltage developed across the 38 kHz emitter decoupling network (pin 14). If this is the case, the mute driving voltage could be made low enough, under the absence of a stereo signal, as to keep the switch in the ON position, muting any monaural station as well as the interstation noise.

The short circuit between Ⓜ and ground decreases the effective emitter resistance in series with Q4, but still provides a high enough load to develop a substantial 19 kHz signal at the input of Q7 (pin 2) if a stereophonic signal is fed to the input. Accordingly, the dc voltage at pin 14 increases, triggering the mute switch OFF. The final result of this combination will be a receiver with a "stereo select" action, able to reject any monaural program automatically. When this combination is being used, the use of a stereo lamp indicator becomes redundant.

Stereo reception is poor when the signal to noise ratio is low, and it is, therefore, desirable to detect weak signals monaurally. Such action is easily obtained automatically by making the dc driving voltage applied to the stereo-monaural switch a fraction of that applied to the mute switch. The voltage divider is designed in such a way that any RF level below a predetermined point considered acceptable, will not provide enough dc voltage to switch the stereo-monaural switch into the stereo mode.

CIRCUIT EVALUATION

The circuit evaluation has been conducted using different levels of composite and pilot signal levels. The circuit used for this purpose is shown in Figure 4. The overall performance of a typical circuit is summarized in Tables I, II, III, IV, V and VI.
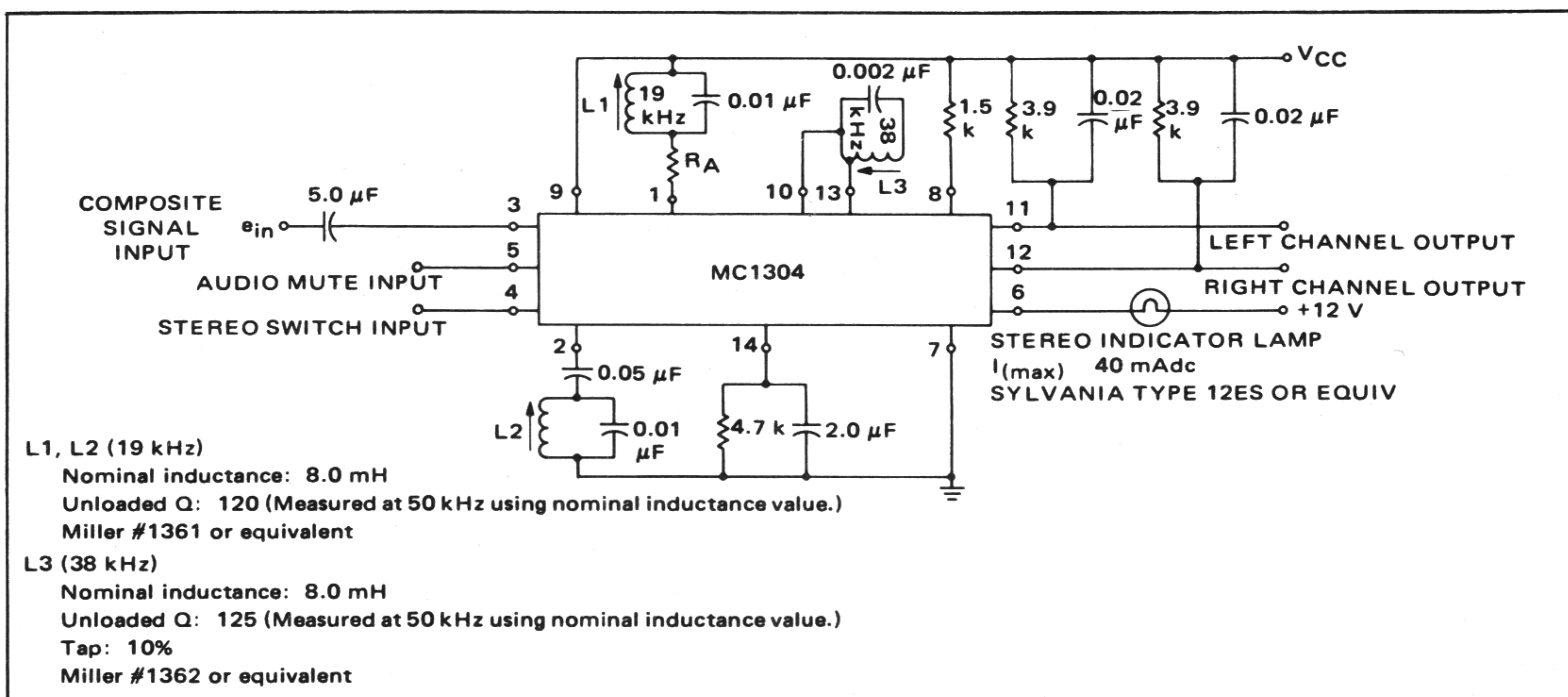

L1, L2 (19 kHz)
    Nominal inductance: 8.0 mH
    Unloaded Q: 120 (Measured at 50 kHz using nominal inductance value.)
    Miller #1361 or equivalent
L3 (38 kHz)
    Nominal inductance: 8.0 mH
    Unloaded Q: 125 (Measured at 50 kHz using nominal inductance value.)
    Tap: 10%
    Miller #1362 or equivalent

FIGURE 4 — Typical Circuit Configuration

TABLE I — Channel Separation versus Frequency

Input signal: 200 mVrms, 10% pilot (L = 1; R = 0 or vice versa)

Frequency	Channel Separation dB	
Hz	R = 1; L = 0	R = 0; L = 1
100	35	36
1000	47	46
10,000	34	35

TABLE II — Ultrasonic Frequency Rejection

(measured with respect to the 1 kHz level)

Input signal: 280 mV peak (L = –R), 10% pilot

Frequency kHz	Attenuation dB
19	31
38	23

TABLE III — 67 kHz SCA Rejection

(measured with respect to the 1 kHz level, without an input trap)

Input signal: 200 mVrms composite signal, 10% pilot adjusted to F.C.C. specs*

SCA Frequency kHz	Frequency By-Products kHz	Attenuation dB
60	3	60
67	9	75
	10	75
74	2	70

*NOTE: 80% composite, 10% pilot; 10% SCA

TABLE IV — Auxiliary Circuits

Mute Switch	Typical Values
Minimum dc voltage to be applied to Pin 5 to turn the Mute OFF	1.5 V
Maximum dc voltage to be applied to Pin 5 to turn the Mute ON	0.7 V

Stereo-Monaural Switch	
Minimum dc voltage to be applied to Pin 4 to have stereo operation	1.5 V
Maximum dc voltage to be applied to Pin 4 to have monaural operation	0.7 V

TABLE V — Channel Separation at 1 kHz versus Temperature

Ambient Temperature	1 kHz Channel* Separation	
°C	dB	
	R	L
25	46	45
55	40	48

*NOTE: Using polystyrene RPJ Centralab capacitors (Tol. ± 10%)

TABLE VI — 1 kHz Channel Separation versus Pilot Level

Pilot Level mVrms	Channel Separation dB
15	42
50	38
100	25

The data sheet on either the MC1304 or 1305 complements the information given above, showing the 19 kHz sensitivity of the unit and the THD performance, for both, the monaural and the stereo mode.

REFERENCE

Popp, D. J. — The study of SCA Interference in Stereo FM Receivers

IEEE Transactions on Broadcast and TV Receivers — July 1963

CIRCUIT CONSIDERATIONS

The incorporation of the MC1304 in an FM receiver calls for two basic considerations:

(A) The selection of the B+ voltages for the IC and lamp indicator.

(B) The derivation of the dc voltages needed to drive the mute and stereo-monaural switches.

A — POWER SUPPLY SELECTION

Two practical situations could occur: (a) The IC is being incorporated in an existing receiver where discrete components are being used; (b) An entirely new design is being worked out.

In the first case the selection of the B+ voltage for the IC and the lamp indicator will be mainly determined by the B+ availability of the receiver while in the case of a new design the gain of the multiplex unit could be the determining factor for the choice of the B+.

In any case, the B+ voltage for the IC should have some degree of regulation to overcome the usual variations on the main voltage (±10%). This regulation is needed because the percentage of THD in the unit is bias dependent. For this reason, independently of the value being chosen for the B+, the voltage between pin 8 and ground (MC1304) should be kept close to 4.6 V. This condition can be easily achieved selecting the proper value for the resistor connected between pin 8 and B+.

If an MC1305 is used instead, the B+ voltage should be 8.5 V because a 2 kilohm resistor (Figure 3) has been integrated on the chip.

The maximum dc current taken by the MC1304, under any B+ condition, never exceeds the 20 mA range.

For the lamp indicator the maximum B+ value is limited to 22 V because no higher voltage between any pin and ground is permitted (see maximum ratings). The type of lamp being used will determine the maximum load in the circuit. Care should be taken not to exceed the 40 mA maximum rating.

The use of separate supplies for the IC and the lamp driver is strongly recommended. This circuit approach simplifies the design of both power supplies and does away with the B+ modulation effect that, otherwise, will be present when switching the lamp indicator ON or OFF.

B — DERIVATION OF THE DC DRIVING VOLTAGES

The stereo lamp driver switch is the only switch that is driven internally. If automatic muting or stereo-monaural selection are required, the dc driving voltage to those circuits will have to be made dependent on the RF incoming signal.
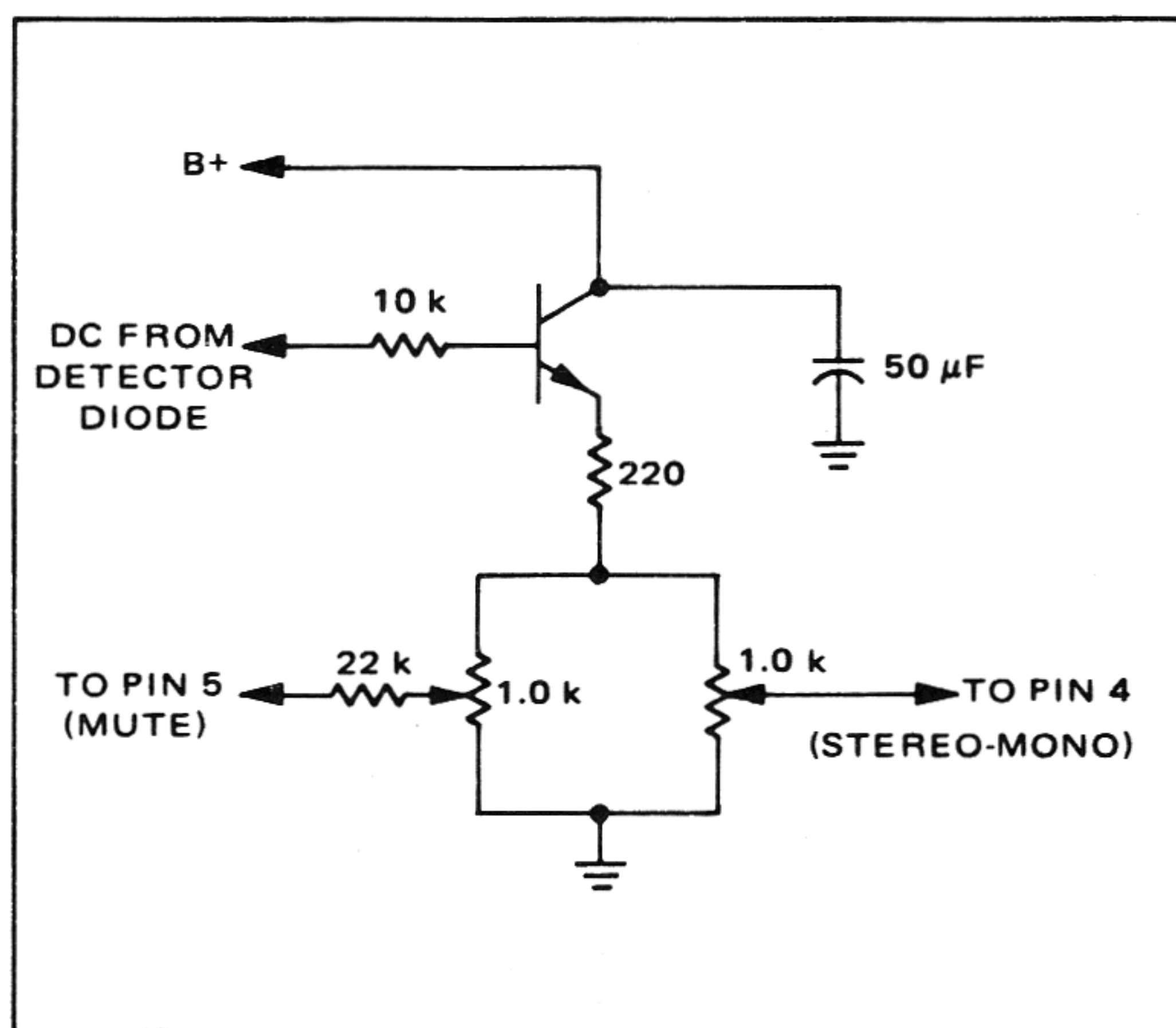
FIGURE 5 — Suggested Emitter Follower Circuit for Driving Voltages of Auxiliary Circuit Functions

Probably the most economical way to achieve this goal is to use the dc voltage available at the output of one of the ratio detector diodes (the one producing a dc voltage positive with respect to ground).

This voltage, due to the presence of filtering capacitances, is fairly immune to noise "spikes", a condition that is highly desirable when driving a Schmitt trigger switch. The only limitation for its usage is generally related to the available dynamic change of this dc voltage.

A minimum of 2:1 is required for the switch circuits. Obtaining the actual values are not usually a problem. The switch will remain in the mute mode if the value of the voltage applied to pin 5 is lower than 0.6 V, and it will change its state if this voltage becomes higher than 1.2 V. If the ratio is available, a voltage divider could be always designed to get the proper values.

In some receivers the sensitivity is too high, limiting the dynamic dc change to a ratio lower than 2:1. If this is the case, a small reduction of the sensitivity will be usually sufficient to improve the dynamic range. In a new design, of course, this problem could be contemplated from the start.

To avoid any loading from the IC, the auxiliary circuits could be isolated from the detector load using an emitter follower such as the one shown in Figure 5. This circuit permits an independent adjustment of the mute and stereo-monaural switches, which is desirable because they act at different RF signal levels.

APPENDIX I

SYNCHRONOUS DETECTOR WITH IMPROVED CHANNEL SEPARATION

To have a better understanding of how the synchronous detector in the MC1304 works, the detector is redrawn in Figure 1A, showing one of the outputs with solid lines and the other with dotted lines.

The pair Q15–Q16 is common to both channels.

Due to the inherent mechanism of a balanced pair, a phase inversion is always present between the two transistors in the pair.

In particular, as Q10 and Q13 are driven in parallel, there is a 180° phase shift between Q12 and Q13. A similar situation occurs between Q15 and Q16, in the lower pair.

The signal developed across R is the sum of two signal products. One is the product of the square wave present at Q13 and the signal present at Q16. The other is the product of the square wave present at Q12 and the signal present at Q15.
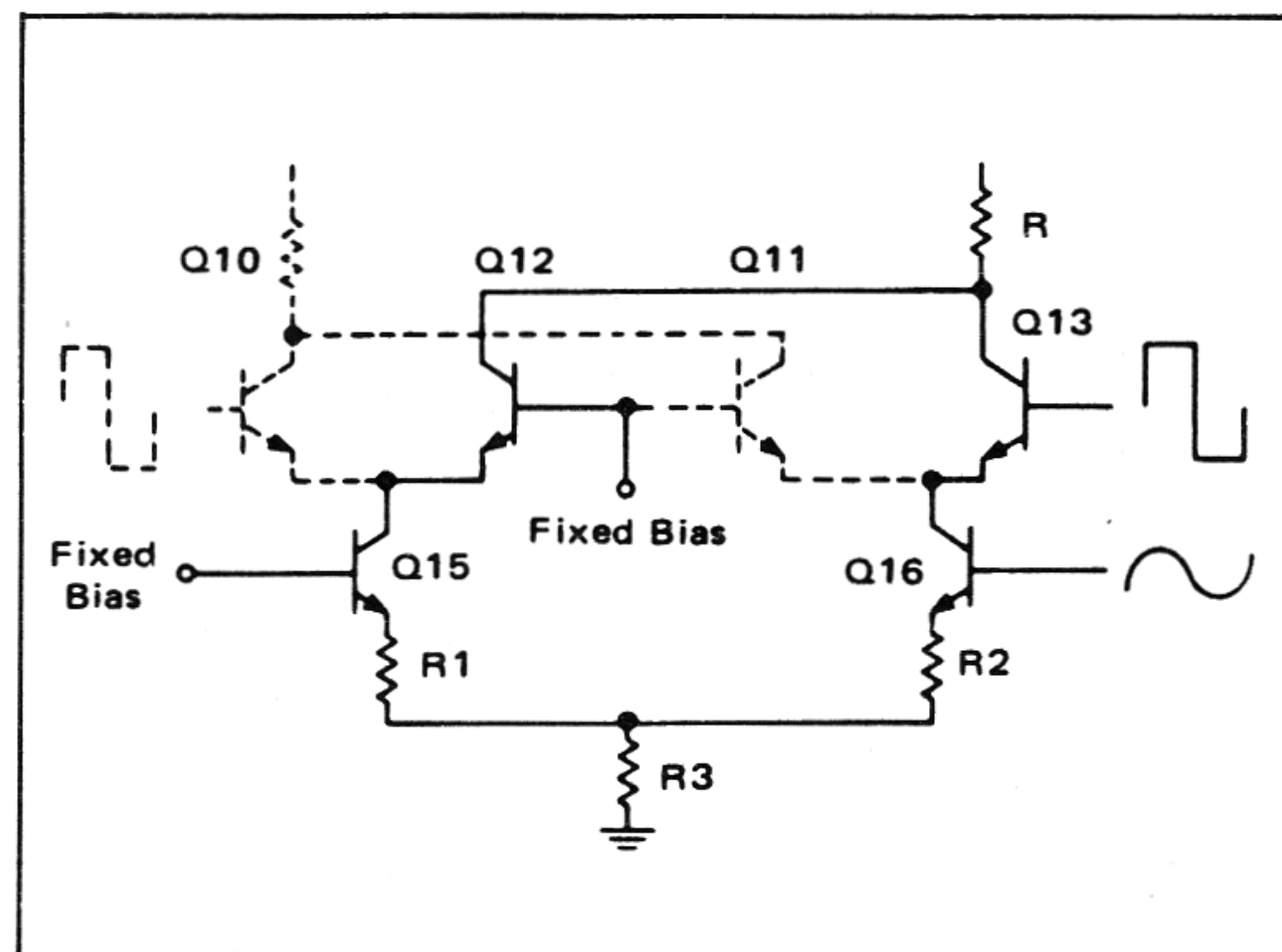

FIGURE 1A — Synchronous Detector

The signal at Q15 will be 180° out of phase with respect to Q16. Only a fraction (k) of the voltage fed to Q15 will be present at Q16, due to the presence of R1, R2, and R3. If both the square wave at Q13 and the composite signal at Q16 are assumed to have the same phase, then

$$V_{out} = \left|(L+R) + (L-R)\cos\omega_{sc}t\right|\left(1 + \frac{4}{\pi}\cos\omega_{sc}t\right)$$
$$-k\left|(L+R) + (L-R)\cos\omega_{sc}t\right|\left(1 - \frac{4}{\pi}\cos\omega_{sc}t\right) \quad (1)$$

where: $\left|k\right| < 1$

If only the audio frequencies are being considered, the former expression becomes:

$$V_{out} = (L+R) + \frac{2}{\pi}(L-R) - k(L+R) + \frac{2k}{\pi}(L-R) \quad (2)$$

$$V_{out} = R\left(1 - \frac{2}{\pi} - k - \frac{2k}{\pi}\right) + L\left(1 + \frac{2}{\pi} - k + \frac{2k}{\pi}\right) \quad (3)$$

As can be seen, the output signal contains not only the wanted left channel information, but some unwanted right channel information. But this remainder is a function of the value given to k. In particular, if

$$1 - \frac{2}{\pi} - k - \frac{2k}{\pi} = 0 \qquad (4)$$

then an optimum value for k that cancels the crosstalk in the detector can be found.

$$k = \frac{\pi - 2}{\pi + 2} \cong 0.221 \qquad (5)$$

Replacing the value given by (5) in expression (3), we can find the value of the output signal:

$$V_{out} = \frac{8L}{2 + \pi} \qquad (6)$$

$$V_{out} = 1.55 \, L \qquad (7)$$

A similar analysis could be done for the other channel.

APPENDIX II
ANALYSIS OF THE MATRIX CIRCUIT

The lower differential pair is redrawn in Figure 2A.

A variation of the incoming signal ($\triangle e_i$) is assumed to take place at the base of Q1. Considering the base of Q2 to be grounded for ac, and disregarding V_{BE} in both transistors, we will have:
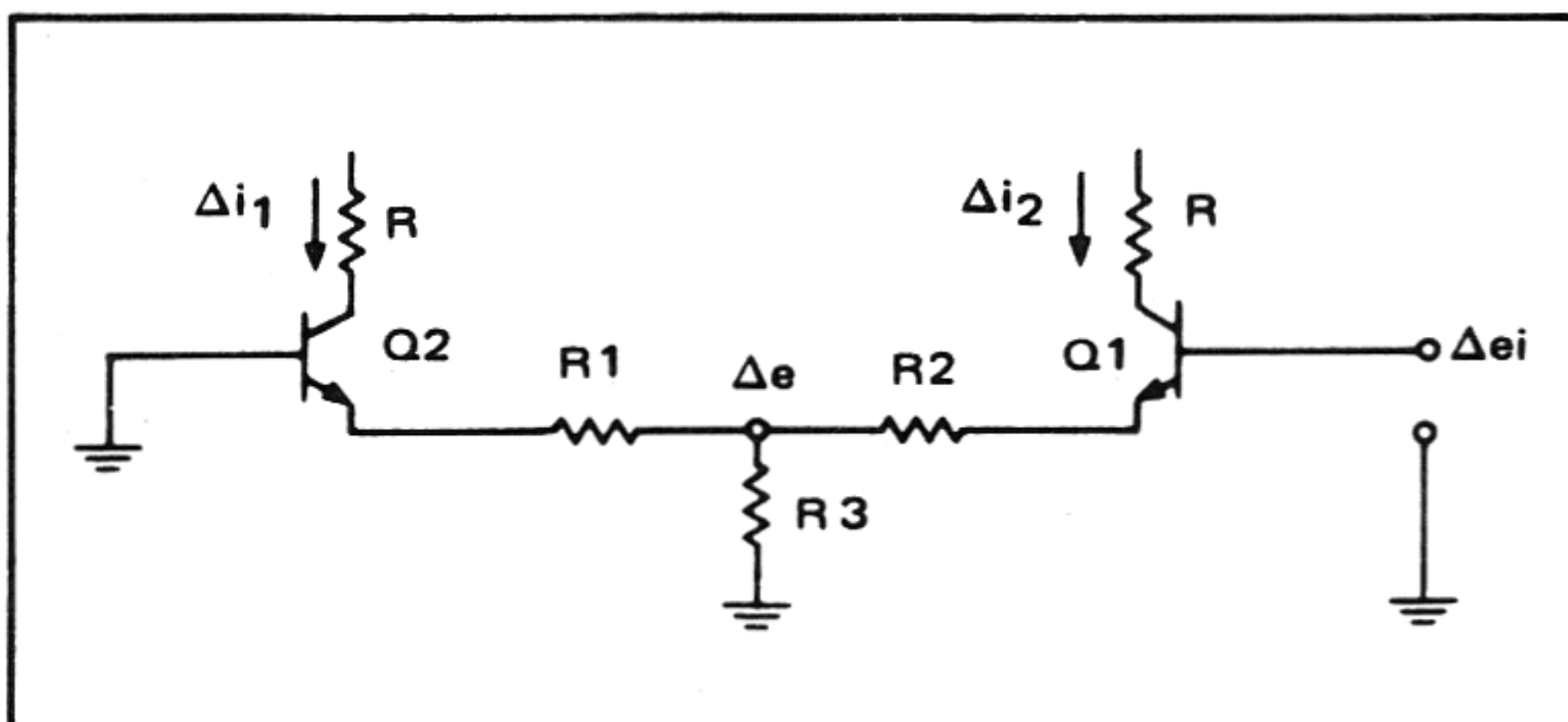

FIGURE 2A — Lower Differential Pair

$$\triangle e = \triangle e_i \cfrac{\cfrac{R_3 R_1}{R_3 + R_1}}{R_2 + \cfrac{R_1 R_3}{R_1 + R_3}}$$

Making

$$\frac{R_3 R_1}{R_3 + R_1} = P$$

and $\qquad R_2 + P = S$

then, $\qquad \triangle e = \triangle e_i \dfrac{P}{S}$

The value of $\triangle i_2$ will be given by

$$\triangle i_2 = \cfrac{\triangle e_i}{R_2 + \cfrac{R_3 R_1}{R_3 + R_1}}$$

or $\qquad \triangle i_2 = \dfrac{\triangle e_i}{S}$

For $\triangle i_1$ the value will be given by

$$\triangle i_1 = \frac{\triangle e}{R_1}$$

Then,

$$\frac{\triangle i_1}{\triangle i_2} = \frac{\triangle e}{R_1} \frac{S}{e_i} = \triangle e_i \frac{P}{S R_1} \frac{S}{\triangle e_i}$$

or

$$\frac{\triangle i_1}{\triangle i_2} = \cfrac{\cfrac{R_3 R_1}{R_3 + R_1}}{R_1} = \frac{R_3}{R_3 + R_1}$$

in our circuit, $R_1 = 1.0 \, k\Omega$

$$R_2 = 1.0 \, k\Omega$$

$$R_3 = 310\Omega \text{ (Three } 930\Omega$$
$$\text{resistors in parallel.)}$$

Then,

$$\frac{\triangle i_1}{\triangle i_2} = \frac{310}{1,310} = 0.236$$

This value is a satisfactory approximation to the value needed for k as described in Appendix I.